PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

SHINTANI et al.

Application No.	Unassigned	Art Unit:	Unassigned
Filed:	August 22, 2001	Examiner:	Unassigned
For:	METHOD OF FABRICATING SEMICONDUCTOR DEVICE AND WAFER TREATMENT APPARATUS EMPLOYED THEREFOR AS WELL AS SEMICONDUCTOR DEVICE		

PENDING CLAIMS AFTER ENTRY OF PRELIMINARY AMENDMENT

1. A method of fabricating a semiconductor device comprising a wafer treatment of a first part of the wafer having a first etching property and a second part of the wafer having a second etching property different from the first etching property, in a chamber with a gas for etching, including:

introducing the gas for etching into the chamber, and

assuming that a time between introduction of the gas for etching into the chamber and starting of etching of the first part of the wafer is a first starting time, and a time between introduction of the gas for etching into the chamber and starting of etching of the second part of the wafer is a second starting time, longer than said first starting time, supplying the gas for etching for a time longer than the first starting time but shorter than the second starting time.

2. The method of fabricating a semiconductor device according to claim 1, wherein the time difference between the first starting time and the second starting time is not more than about 5 seconds.

3. The method of fabricating a semiconductor device according to claim 1, further comprising:

forming a gate insulating film on the semiconductor substrate, and

forming a gate electrode on the insulating film, wherein the first part of the wafer contains a reaction product generated before forming the gate electrode, covering the gate insulating film and the gate electrode,

the second part includes said gate insulating film, and

the gas for etching includes hydrofluoric acid.

4. The method of fabricating a semiconductor device according to claim 1, including introducing a reaction accelerating gas into the chamber before introducing the gas for etching for reducing the first starting time.

5. The method of fabricating a semiconductor device according to claim 4, including alternately introducing the reaction accelerating gas and the gas for etching.

6. The method of fabricating a semiconductor device according to claim 4, including continuously adding the reaction accelerating gas after starting supply of the gas for etching.

7. The method of fabricating a semiconductor device according to claim 1, including evacuating the chamber, but not while the gas for etching is being supplied.

8. The method of fabricating a semiconductor device according to claim 1, further comprising:

forming a conductive layer on a gate insulating film on the semiconductor substrate,

forming a layer for defining a mask on the conductive layer,

etching the conductive layer through a mask of the layer for defining a mask, thereby forming a gate electrode, and

removing the layer for defining a mask remaining on the gate electrode after formation of the gate electrode, wherein

the first part of the wafer includes the layer for defining a mask,

the second part of the wafer includes the gate insulator film, and

hydrofluoric acid gas is supplied as the gas for etching to remove the layer for defining a mask.

9. The method of fabricating a semiconductor device according to claim 8, including repeatedly supplying the gas for etching.

10. The method of fabricating a semiconductor device according to claim 9, including evacuating the chamber, and alternatively supplying the gas for etching and evacuating the chamber.

11. A wafer treatment apparatus for treating a first part of the wafer having a first etching property and a second part of the wafer having a second etching property, different from the first etching property with a gas for etching, comprising:

a chamber for holding a wafer;

an etching gas supply part supplying the gas for etching into said chamber; and

a control part controlling supply of the gas for etching from said etching gas supply part into said chamber, wherein said control part, assuming that a time between introduction of the gas for etching into said chamber and starting of etching of the first part of the wafer is a first starting time and a time between introduction of the gas for etching into said chamber and starting of etching of the second part of the wafer is a second starting time, longer than the first starting time, supplies the gas for etching from said etching gas supply part into said chamber for a time longer than the first starting time but shorter than the second starting time.

12. The wafer treatment apparatus according to claim 11, wherein the time difference between the first starting time and the second starting time is not more than about 5 seconds.

13. The wafer treatment apparatus according to claim 11, further comprising an added gas supply part supplying a reaction accelerating gas, for reducing the first starting time, into said chamber, wherein said control part supplies the reaction accelerating gas from said added gas supply part into said chamber before supplying the gas for etching.

14. The wafer treatment apparatus according to claim 13, wherein said control part alternately supplies the gas for etching and the reaction accelerating gas.

15. The wafer treatment apparatus according to claim 13, wherein said control part supplies the reaction accelerating gas while supplying the gas for etching.

16. The wafer treatment apparatus according to claim 11, further comprising an evacuation part evacuating said chamber, wherein said control part prevent said evacuation part from operating while supplying the etching gas.

17. A method of cleaning a wafer after formation of a gate electrode, including removing a reaction product formed by etching with hydrofluoric acid gas, after forming the gate electrode that has been patterned by the etching with a mask on a semiconductor substrate, through a gate insulating film.

18. The cleaning method according to claim 17, including removing the reaction product with hydrofluoric acid gas within a reaction time difference between a time when the reaction product is etched by the hydrofluoric acid gas and a time when the gate insulating film is etched by the hydrofluoric acid gas.

19. The cleaning method according to claim 18, wherein the reaction time difference is repetitively set, thereby removing the reaction product with the hydrofluoric acid gas.

20. The cleaning method according to claim 19, wherein a semiconductor substrate including the gate electrode is set in a chamber, and the reaction time difference is repetitively set by repeatedly evacuating the chamber and charging the chamber with the hydrofluoric acid gas.